AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 4, line 1, with the following rewritten paragraph:

-- The method for fabricating trench isolations provided in the invention includes the following steps. First, a semiconductor substrate with a trench is provided, and a first dielectric layer is formed on the substrate and fills the trench by LPCVD. Next, the first dielectric layer is etched, so that its surface is lowered [[to]] below the opening of the trench. Subsequently, a second dielectric layer is formed on the first dielectric layer by ~~HPCVD~~ HDPCVD. Then, the second dielectric layer is planarized by CMP. Finally, a rapid thermal annealing procedure is performed.

Please replace the paragraph beginning on page 4, line 12, with the following rewritten paragraph:

-- The present invention combines both LPCVD and ~~HPCVD~~ HDPCVD with adequate process sequence and conditions. The advantages of this combination are described in the following. The invention eliminates the complicated and expensive multiple deposition and etching cycles required by conventional ~~HPCVD~~ HDPCVD, thus simplifying the process and reducing the cost thereof. A second dielectric layer with superior dielectric characteristics is deposited on the first dielectric layer, so that the lengthy conventional annealing can be replaced by a rapid thermal annealing procedure, thus improving the characteristics of the second dielectric layer. The anisotropic etching and wet etching using hydrogen fluoride lower the surface of the first dielectric layer, by a specific height, to the opening of the trench, thus filling voids near the opening of the trench and providing improved gap-filling properties.

Please replace the paragraph beginning on page 4, line 29, with the following rewritten paragraph:

-- Another method for fabricating trench isolations provided in the invention includes the following steps. First, a semiconductor substrate with a first trench with a relatively high aspect

ratio and a second trench with a relatively low aspect ratio is provided, and a first dielectric layer is formed on the substrate and fills both trenches by LPCVD. Next, the first dielectric layer is etched, and its surface is lowered by a specific height [[to]] below the opening of the first trench, and a spacer is formed simultaneously on the sidewalls of the second trench. A second dielectric layer is subsequently formed on the first dielectric layer by ~~HPCVD~~ HDPCVD. The second dielectric layer is then planarized by CMP. Finally, a rapid thermal annealing procedure is performed. In addition to the above advantages, the method of the present invention is also suitable for fabricating elements having trenches with different aspect ratios, such as SOC (system on a chip) or 100 nm DRAM.

Please replace the paragraph beginning on page 7, line 10, with the following rewritten paragraph:

– FIG. 2C illustrates the etching step, including anisotropic etching such as RIE or plasma etching and the wet etching using hydrogen fluoride, wherein hydrogen fluoride is a diluted solution, with a concentration ratio of 200:1. After etching, the surface of the first dielectric layer 107 is lowered by about 100~1000Å [[to]] below the opening of the first trench 103, and the first dielectric layer 107 forms a spacer 109 on the sidewalls of the second trench 104 simultaneously.